

1     WHAT IS CLAIMED IS

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1. A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal, said semiconductor device comprising:

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address-latch circuits which latches the addresses;

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a first control circuit which selects one of said address-latch circuits in sequence in response to the clock signal, and controls the selected one of said address-latch circuits to latch a corresponding one of the addresses in response to the clock signal; and

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a second control circuit which selects one of said address-latch circuits in sequence in response to the strobe signal, and controls the selected one of said address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

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2. The semiconductor device as claimed in claim 1, further comprising data-latch circuits, each of which latches a corresponding datum of the data in synchronism with the strobe signal, and outputs the corresponding datum of the data in synchronism with the strobe signal.

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3. The semiconductor device as claimed in

1 claim 2, wherein said data-latch circuits operate in  
response to a write-enable signal which is generated  
in response to a write command to said semiconductor  
device.

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4. The semiconductor device as claimed in  
10 claim 3, wherein the write-enable signal controls said  
first control circuit and said second control circuit  
to operate for a predetermined time period after  
receiving the write command.

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5. The semiconductor device as claimed in  
claim 1, wherein said first control circuit includes a  
20 first frequency divider configured to divide a  
frequency of the clock signal, and selects one of said  
address-latch circuits in sequence by using the  
frequency-divided clock signal from said first  
frequency divider, and said second control circuit  
25 includes a second frequency divider configured to  
divide a frequency of the strobe signal, and selects  
one of said address-latch circuits in sequence by  
using the frequency-divided clock signal from said  
second frequency divider.

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6. The semiconductor device as claimed in  
35 claim 1, further comprising:

an increment-latch circuit which latches one  
of the addresses in synchronism with the clock signal;

1 and  
an address-generation circuit which  
increments the one of the addresses latched by said  
increment-latch circuit by 1, and supplies the  
5 incremented address to said address-latch circuits,  
wherein each of said address-latch circuits  
configured so as to be capable of selecting the  
corresponding one of the addresses externally provided  
or the incremented address supplied from said address-  
10 generation circuit for the latching operation thereof.

15 7. The semiconductor device as claimed in  
claim 2, wherein said data-latch circuit comprises:  
a first data-latch circuit which latches a  
corresponding datum of the data in synchronism with a  
rising edge of the strobe signal; and  
20 a second data-latch circuit which latches a  
corresponding datum of the data in synchronism with a  
falling edge of the strobe signal.

25 8. A semiconductor device which receives  
addresses in synchronism with a clock signal and  
receives data in synchronism with a strobe signal,  
30 said semiconductor device comprising:  
data-latch circuits;  
a first control circuit which selects one of  
said data-latch circuits in sequence in response to  
the strobe signal, and controls the selected one of  
35 said data-latch circuits to latch a corresponding  
datum of the data in response to the strobe signal;  
and

1           a second control circuit which selects one  
of said data-latch circuits in sequence in response to  
the clock signal, and controls the selected one of  
said data-latch circuits to output a corresponding  
5 datum of the data in response to the clock signal.

10           9. The semiconductor device as claimed in  
claim 8, further comprising an address-latch circuit  
which latches the addresses in sequence in synchronism  
with the clock signal, and outputs the addresses in  
synchronism with the clock signal.

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20           10. The semiconductor device as claimed in  
claim 8, wherein said address-latch circuit operates  
in response to a write-enable signal which is  
generated in response to a write command to said  
semiconductor device.

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30           11. The semiconductor device as claimed in  
claim 10, wherein the write-enable signal controls  
said first control circuit and said second control  
circuit to operate for a predetermined time period  
after receiving the write command.

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12. The semiconductor device as claimed in

1 claim 8, wherein said first control circuit includes a  
first frequency divider configured to divide a  
frequency of the strobe signal, and selects one of  
said data-latch circuits in sequence by using the  
5 frequency-divided strobe signal from said first  
frequency divider, and said second control circuit  
includes a second frequency divider configured to  
divide a frequency of the clock signal, and selects  
one of said data-latch circuits in sequence by using  
10 the frequency-divided clock signal from said second  
frequency divider.

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13. The semiconductor device as claimed in  
claim 9, further comprising  
an address-generation circuit which  
increments one of the addresses latched by said  
20 address-latch circuit, and supplies the incremented  
address to said address-latch circuit,  
wherein said address-latch circuit is  
configured so as to be capable of selecting the  
addresses externally provided or the incremented  
25 address supplied from said address-generation circuit  
for the latching operation thereof.

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14. The semiconductor device as claimed in  
claim 8, wherein each of said data-latch circuits  
includes:  
a first latch which latches a corresponding  
35 datum of the data in synchronism with a rising edge of  
the strobe signal; and  
a second latch which latches a corresponding

1 datum of the data in synchronism with a falling edge  
of the strobe signal.

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15. The semiconductor device as claimed in  
claim 9, wherein said address-latch circuit includes a  
delay circuit which delays output timings of the  
10 addresses by a predetermined number of cycles of the  
clock signal.

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16. The semiconductor device as claimed in  
claim 1, further comprising an address buffer, wherein  
said address-latch circuits supply the addresses to  
said address buffer without a clock-cycle delay during  
20 a read operation.

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17. The semiconductor device as claimed in  
claim 9, further comprising an address buffer, wherein  
said address-latch circuit supplies the addresses to  
said address buffer without a clock-cycle delay during  
a read operation.

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18. A memory circuit, comprising:  
35 an address-input circuit which latches  
address signals in response to a clock signal, and  
outputs the address signals in response to a timing

1 ~~signal;~~

a data-input circuit which latches data  
signals in response to a strobe signal, and outputs  
the data signals in response to the timing signal; and  
5 an internal circuit which writes the data  
signals supplied from the data-input circuit in memory  
cells indicated by the address signals supplied from  
the address-input circuit.

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19. The memory circuit as claimed in claim  
18, wherein said timing signal is responsive to the  
15 strobe signal.

20 20. The memory circuit as claimed in claim  
18, wherein said timing signal is responsive to the  
clock signal.

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21. The memory circuit as claimed in claim  
18, wherein the strobe signal has a cycle identical to  
that of the clock signal, and a first timing of a  
30 first rising edge of the strobe signal is different  
from a second timing of a corresponding rising edge of  
the clock signal.

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22. The memory circuit as claimed in claim

1     21, wherein the first timing is later than the second  
timing with a timing gap therebetween being shorter  
than one cycle of the clock signal.

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23. The memory circuit as claimed in claim  
18, wherein said data-input circuit latches the data  
signals in synchronism with rising edges and falling  
10 edges of the strobe signal.

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24. The memory circuit as claimed in claim  
19, wherein the address-input circuit includes:

a first latch circuit which latches the  
address signal in response to a first rising edge of  
the clock signal, and outputs the address signal in  
20 response to the timing signal; and

a second latch circuit, connected in  
parallel to the first latch circuit, which latches  
next address signal in response to a next rising edge  
of the clock signal, and outputs the next address  
25 signal in response to the timing signal.

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25. The memory circuit as claimed in claim  
24, wherein the address-input circuit outputs the  
address signal prior to outputting the next address  
signal.

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1           26. The memory circuit as claimed in claim  
19, further comprising:

5           a decode circuit which receives the address  
signal from the address-input circuit, and decodes the  
address signal in response to a first activation  
signal; and

10           a write amplifier which receives the data  
signal from the data-input circuit, and amplifies the  
data signal in response to a second activation signal  
in a data-write mode,

          wherein both of the first and second  
activation signals are responsive to the strobe signal  
in the data-write mode.

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20           27. The memory circuit as claimed in claim  
26, wherein in a data-read mode, the first activation  
signal is responsive to the clock signal, and the  
second activation signal is in a deactivated state.

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20           28. The memory circuit as claimed in claim  
20, wherein said data-input circuit includes:

30           a first data-input circuit which latches the  
data signals in sequence in response to a first rising  
edge and a first falling edge of the strobe signal,  
and outputs the data signals in parallel in response  
to the timing signal; and

35           a second data-input circuit, connected in  
parallel to the first data-input circuit, which  
latches next data signals in sequence in response to a  
next rising edge and a next falling edge of the strobe  
signal, and outputs the next data signals in parallel

1 in response to the timing signal.

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29. The memory circuit as claimed in claim 20, wherein said data-input circuit includes a first data-input circuit which latches the data signals in sequence in response to a rising edge and a falling edge of the strobe signal, and outputs the data signals in parallel in response to the timing signal.

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30. The memory circuit as claimed in claim 29, wherein said first data-input circuit latches next data signals after outputting the data signals.

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31. The memory circuit as claimed in claim 28, wherein said data-input circuit outputs the data signals prior to outputting the next data signals.

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32. The memory circuit as claimed in claim 20, wherein said address-input circuit includes a shift register which operates in response to the clock signal.

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1           33. The memory circuit as claimed in claim  
19, wherein said address-input circuit includes a  
shift register which operates in response to the clock  
signal.

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10           34. A method of writing data in the memory  
circuit of claim 33, comprising a step of adjusting an  
input timing of the strobe signal relative to the  
clock signal such that said shift register stores two  
addresses at a time when the data-input circuit  
outputs the data signals.

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20           35. The memory circuit as claimed in claim  
20, further comprising:

a decode circuit which receives the address  
signal from the address-input circuit, and decodes the  
address signal in response to a first activation  
signal; and

25           a write amplifier which receives the data  
signal from the data-input circuit, and amplifies the  
data signal in response to a second activation signal  
in a data-write mode,

30           wherein both of the first and second  
activation signals are responsive to the clock signal  
in the data-write mode.

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36. The memory circuit as claimed in claim  
35, wherein in a data-read mode, the first activation

1 signal is responsive to the clock signal, and the  
second activation signal is in a deactivated state.

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37. The memory circuit as claimed in claim  
26, wherein in the data-write mode, the first  
activation signal activates said decode circuit after  
10 said address-input circuit outputs the address  
signals, and the second activation signal activates  
said write amplifier after said data-input circuit  
outputs the data signals.

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38. The memory circuit as claimed in claim  
35, wherein in the data-write mode, the first  
20 activation signal activates said decode circuit after  
said address-input circuit outputs the address  
signals, and the second activation signal activates  
said write amplifier after said data-input circuit  
outputs the data signals.

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39. The memory circuit as claimed in claim  
30 32, wherein said shift register delays the address  
signals by 1.5 clock cycles of the clock signal.

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40. The memory circuit as claimed in claim  
18, wherein a timing at which said address-input

1 circuit outputs the address signals is concurrent with  
a timing at which said data-input circuit outputs the  
data signals corresponding to the address signals.

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41. The memory circuit as claimed in claim  
32, further comprising a bypass circuit provided in  
10 parallel to said shift register, wherein the address  
signals pass through the bypass circuit and bypass  
said shift register in a data-read mode.

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42. The memory circuit as claimed in claim  
33, further comprising a bypass circuit provided in  
parallel to said shift register, wherein the address  
20 signals pass through the bypass circuit and bypass  
said shift register in a data-read mode.

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